RDK X3 Module Design Guide

v1.0

Chapter 1. Introduction

1.1 References

Refer to the following list of documents or models for more information. Use the latest revision of all documents.

RDK X3 Module Datasheet
RDK X3 Module Pinmux
RDK X3 Module Thermal Design Guide
RDK X3 Module AVL (Approved Validation List)

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the interfaces supported by the RDK X3 Module.

1.2 Abbreviations and Definitions

Table 1-1 lists the abbreviations that may be used throughout this design and guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CSI	Camera Serial Interface
Diff	Differential
ESD	Electrostatic Discharge
EMI	Electromagnetic Interference
FET	Field Effect Transistor
GPIO	General Purpose Input Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I2C	Inter IC Interface
I2S	Inter IC Sound Interface

LDO	Low Dropout (voltage regulator)
LPDDR4	Low Power Double Data Rate DRAM, Forth generation
MDI	Medium-Dependent Interface
MIPI	Mobile Industry Processor Interface
mm	Millimeter
ms	Milliseconds

Abbreviation	Definition
PHY	Physical Interface (that is, USB PHY)
ps	Pico-Seconds
PMIC	Power Management In RDK X3 Module Circuit
RJ45	8P8C modular connector used in Ethernet and other data links
RTC	Real Time Clock
SE	Single-Ended
SoC	System on Chip
SPI	Serial Peripheral Interface
TMDS	Transition-Minimized Differential Signaling
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
MIPI	Mobile Industry Processor Interface
eMMC	embedded MultiMediaCard
SDIO	Secure Digital Input and Output

Chapter 2. RDK X3 Module

The RDK X3 Module resides at the center of the embedded system solution and includes:
- Power (Power sequencer, regulators, and so on)
- DRAM (LPDDR4)
- Gigabit Ethernet PHY
- QSPI NAND (Boot device)
- eMMC 5.0 (Storage device, Optional)
- Wi-Fi&BLE (Optional)

In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown in Table 2-1 and Figure 2-1.

Table 2-1. RDK X3 Module Interfaces

Category	Function	Category	Function
USB	USB 3.0 (1x)	LAN	Gigabit Ethernet (1x)
		WLAN	IEEE 802.11a/b/g/n/ac
SDIO	Micro SD (1x)	Bluetooth	BLE 4.2
Camera	MIPI-CSI (1x4 lanes and 2x2 lanes)	GPIO	32x
	Control, clock	Main Power	5V DC 3A
Display	HDMI x1		
	MIPI-DSI (1x4 lanes)		

Figure 2-1. RDK X3 Module Block Diagram

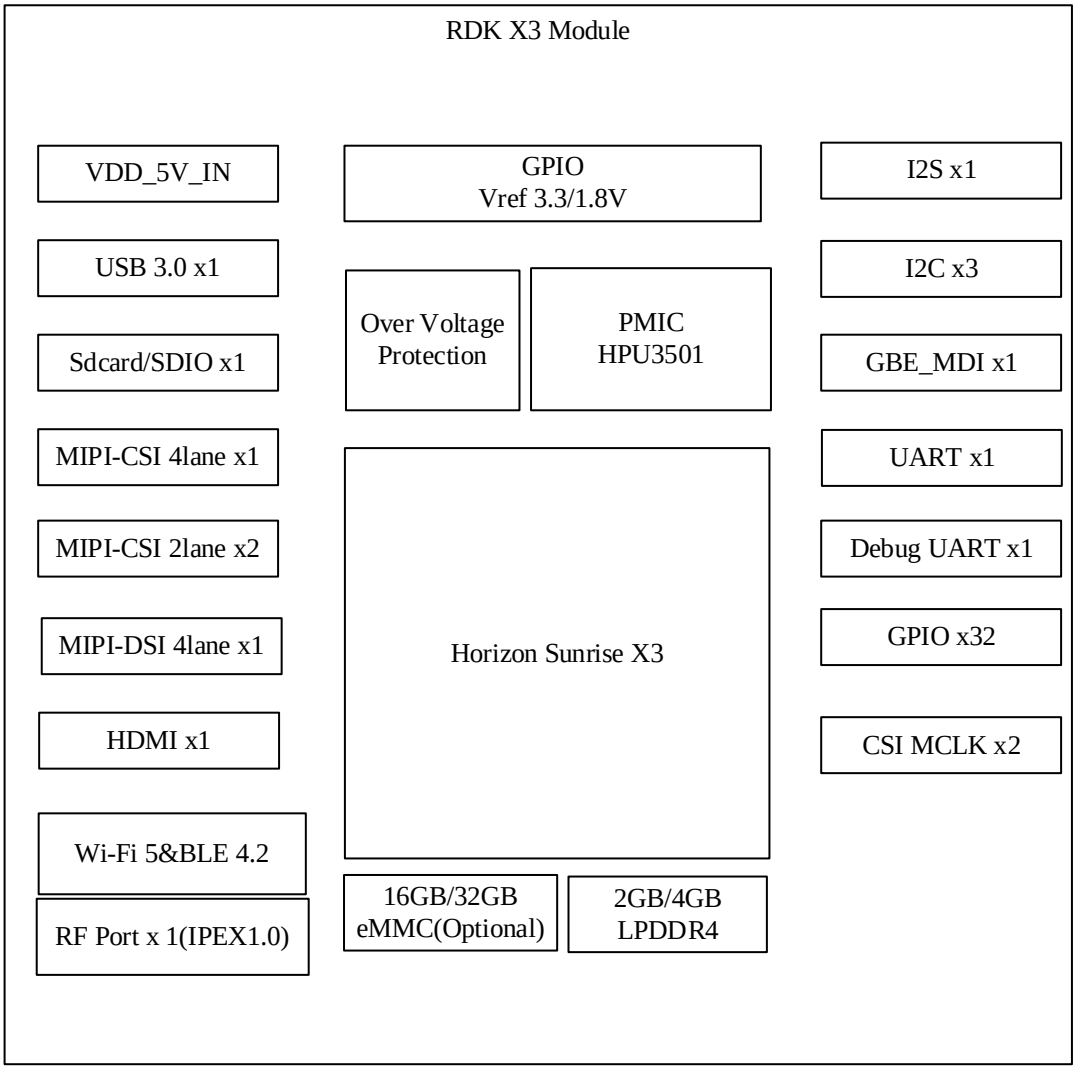


Table 2-2. RDK X3 Module Connector 200-Pin Pinout Matrix

Pin	Signal	Description
1	GND	Ground (0V)
2	GND	Ground (0V)
3	Ethernet_Pair3_P	Ethernet pair 3 positive (connect to transformer or MagJack)

4	Ethernet_Pair1_P	Ethernet pair 1 positive (connect to transformer or MagJack)
5	Ethernet_Pair3_N	Ethernet pair 3 negative (connect to transformer or MagJack)
6	Ethernet_Pair1_N	Ethernet pair 1 negative (connect to transformer or MagJack)
7	GND	Ground (0V)
8	GND	Ground (0V)
9	Ethernet_Pair2_N	Ethernet pair 2 negative (connect to transformer or MagJack)
10	Ethernet_Pair0_N	Ethernet pair 0 negative (connect to transformer or MagJack)
11	Ethernet_Pair2_P	Ethernet pair 2 positive (connect to transformer or MagJack)
12	Ethernet_Pair0_P	Ethernet pair 0 positive (connect to transformer or MagJack)
13	GND	Ground (0V)
14	GND	Ground (0V)
15	Ethernet_nLED3	Active-low Ethernet speed indicator (3.3V signal): typically a yellow LED is connected to this pin. A low state indicates the 1Gbit or 100Mbit link: IOL = 8mA @ VOL < 0.4V
16	Debug_Uart0_RX	Uart Data RX pin:Debug,a 1.8V signal
17	Ethernet_nLED2	Active-low Ethernet speed indicator (3.3V signal): typically a yellow LED is connected to this pin. A low state indicates the 1Gbit or 100Mbit link: IOL = 8mA @ VOL < 0.4V
18	Debug_Uart0_TX	Uart Data TX pin:Debug,a 1.8V signal
19	NC	
20	NC	NC
21	Pi_nLED_Activity	Active-low Pi activity LED. 20mA Max 5V tolerant (VOL < 0.4V).
22	GND	Ground (0V)
23	GND	Ground (0V)
24	GPIO26	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
25	GPIO21	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
26	GPIO19	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
27	GPIO20	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
28	GPIO13	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
29	GPIO16	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
30	GPIO6	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
31	GPIO12	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
32	GND	Ground (0V)
33	GND	Ground (0V)
34	GPIO5	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
35	ID_SC	(BCM2711 GPIO 1) GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
36	ID_SD	(BCM2711 GPIO 0) GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
37	GPIO7	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
38	GPIO11	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
39	GPIO8	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
40	GPIO9	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
41	GPIO25	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V

42	GND	Ground (0V)
43	GND	Ground (0V)
44	GPIO10	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
45	GPIO24	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
46	GPIO22	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
47	GPIO23	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
48	GPIO27	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
49	GPIO18	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
50	GPIO17	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
51	GPIO15	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
52	GND	Ground (0V)
53	GND	Ground (0V)
54	GPIO4	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
55	GPIO14	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V
56	GPIO3	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 1.8kΩ pull up to GPIO_VREF
57	SD_CLK	SD card clock signal
58	GPIO2	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO_VREF to 1.8V. Internal 1.8kΩ pull up to GPIO_VREF
59	GND	Ground (0V)
60	GND	Ground (0V)
61	SD_DAT3	SD card/eMMC Data3 signal
62	SD_CMD	SD card/eMMC Command signal
63	SD_DAT0	SD card/eMMC Data0 signal
64	UART2_TXD	Uart Data TX pin: Internal 4kΩ pull up to GPIO_VREF
65	GND	Ground (0V)
66	GND	Ground (0V)
67	SD_DAT1	SD card/eMMC Data1 signal
68	UART2_RXD	Uart Data RX pin: Internal 4kΩ pull up to GPIO_VREF
69	SD_DAT2	SD card/eMMC Data2 signal
70	SENSOR0_MCLK	GPIO: typically a 1.8V signal
71	GND	Ground (0V)
72	SENSOR1_MCLK	GPIO: typically a 1.8V signal
73	NC	NC
74	GND	Ground (0V)
75	SD_PWR_ON	Output to power-switch for the SD card. The module sets this pin high (3.3V) to signal that power to the SD card should be turned on. Defaults Output low. If booting from the SD card is required then a pullup should also be fitted so the power-switch defaults to on.
76	SD0_DET_N	GPIO: typically a 1.8V signal
77	+5V (Input)	4.75V-5.25V. Main power input
78	GPIO_VREF	Must be connected to MD_3.3V (pins 84 and 86) for 3.3V GPIO or MD_1.8V (pins 88 and 90) for 1.8V GPIO. This pin cannot be floating or connected to ground.

79	+5V (Input)	4.75V-5.25V. Main power input
80	SCL1	I2C clock pin: typically used for Camera and Display. Internal 4kΩ pull up to MD_3.3V
81	+5V (Input)	4.75V-5.25V. Main power input
82	SDA1	I2C Data pin: typically used for Camera and Display. Internal 4kΩ pull up to MD_3.3V
83	+5V (Input)	4.75V-5.25V. Main power input
84	MD_3.3V (Output)	3.3V ± 2.5%. Power Output max 300mA per pin for a total of 600mA. This will be powered down during power-off or GLOBAL_EN being set low
85	+5V (Input)	4.75V-5.25V. Main power input
86	MD_3.3V (Output)	3.3V ± 2.5%. Power Output max 300mA per pin for a total of 600mA. This will be powered down during power-off or GLOBAL_EN being set low
87	+5V (Input)	4.75V-5.25V. Main power input
88	MD_1.8V (Output)	1.8V ± 2.5%. Power Output max 300mA per pin for a total of 600mA. This will be powered down during power-off or GLOBAL_EN being set low
89	WL_nDisable	Can be left floating; if driven low the wireless interface will be disabled. Internally pulled up via 4kΩ to 3.3V
90	MD_1.8V (Output)	1.8V ± 2.5%. Power Output max 300mA per pin for a total of 600mA. This will be powered down during power-off or GLOBAL_EN being set low
91	BT_nDisable	Can be left floating; if driven low the Bluetooth interface will be disabled. Internally pulled up via4kΩ to 3.3V
92	RUN_PG	Bidirectional pin. Can be driven low (via a 220Ω resistor) to reset the CPU. As an output, a high signals that power is good and CPU is running. Internally pulled up to 3.3V via 2kΩ
93	nRPIBOOT	A low on this pin forces booting from an RPI server (e.g. PC or a Raspberry Pi); if not used leave floating. Internally pulled up via 4kΩ to 3.3V
94	NC	NC
95	PI_LED_nPWR	Active-low output to drive Power On LED. This signal needs to be buffered.
96	NC	NC
97	Camera_GPIO	Typically used to shut down the camera to reduce power. Reassigning this pin to another function isn’t recommended. MD_3.3V signaling
98	GND	Ground (0V)
99	GLOBAL_EN	Input. Drive low to power off Module. Internally pulled up with a 47kΩ to +5V
100	nEXTRST	Output. Driven low during reset; Driven high (MD_3.3V) once Module CPU has started to boot. Internally pulled up via4kΩ to 3.3V
101	USB_OTG_ID	Input (3.3V signal) USB OTG Pin. Internally pulled up 4K to 3V3. When grounded the Module becomes a USB host but the correct OS driver also needs to be used
102	NC	NC
103	USB_N	USB D-
104	5V	4.75V-5.25V. Main power input
105	USB_P	USB D+
106	5V	4.75V-5.25V. Main power input
107	GND	Ground (0V)
108	GND	Ground (0V)
109	NC	NC
110	NC	NC

111	NC	NC
112	NC	NC
113	GND	Ground (0V)
114	GND	Ground (0V)
115	CAM1_D0_N	Input Camera1 D0 negative
116	USB_RX_P	USB3.0 RX positive
117	CAM1_D0_P	Input Camera1 D0 positive
118	USB_RX_N	USB3.0 RX negative
119	GND	Ground (0V)
120	GND	Ground (0V)
121	CAM1_D1_N	Input Camera1 D1 negative
122	USB_TX_P	USB3.0 TX positive
123	CAM1_D1_P	Input Camera1 D1 positive
124	USB_TX_N	USB3.0 TX negative
125	GND	Ground (0V)
126	GND	Ground (0V)
127	CAM1_C_N	Input Camera1 clock negative
128	CAM0_D0_N	Input Camera0 D0 negative
129	CAM1_C_P	Input Camera1 clock positive
130	CAM0_D0_P	Input Camera0 D0 positive
131	GND	Ground (0V)
132	GND	Ground (0V)
133	CAM1_D2_N	Input Camera1 D2 negative
134	CAM0_D1_N	Input Camera0 D1 negative
135	CAM1_D2_P	Input Camera1 D2 positive
136	CAM0_D1_P	Input Camera0 D1 positive
137	GND	Ground (0V)
138	GND	Ground (0V)
139	CAM1_D3_N	Input Camera1 D3 negative
140	CAM0_C_N	Input Camera0 clock negative
141	CAM1_D3_P	Input Camera1 D3 positive
142	CAM0_C_P	Input Camera0 clock positive
143	NC	NC
144	GND	Ground (0V)
145	NC	NC
146	NC	NC
147	NC	NC
148	NC	NC
149	NC	NC
150	GND	Ground (0V)
151	HDMI0_CEC	Input HDMI0 CEC. 5V tolerant (It can be connected directly to a HDMI connector; a small amount of ESD protection is provided on the Module by an on-board HDMI05-CL02F3)

152	NC	NC
153	HDMI0_HPD	Input HDMI0 hot plug. 5V tolerant. (It can be connected directly to a HDMI connector; a small amount of ESD protection is provided on the Module by an on-board HDMI05-CL02F3)
154	NC	NC
155	GND	Ground (0V)
156	GND	Ground (0V)
157	CAM2_D0_N	Input Camera2 D0 negative
158	NC	NC
159	CAM2_D0_P	Input Camera2 D0 positive
160	NC	NC
161	GND	Ground (0V)
162	GND	Ground (0V)
163	CAM2_D1_N	Input Camera2 D1 negative
164	NC	NC
165	CAM2_D1_P	Input Camera2 D1 positive
166	NC	NC
167	GND	Ground (0V)
168	GND	Ground (0V)
169	CAM2_C_N	Input Camera2 clock negative
170	HDMI0_TX2_P	Output HDMI0 TX2 positive
171	CAM2_C_P	Input Camera2 clock positive
172	HDMI0_TX2_N	Output HDMI0 TX2 negative
173	GND	Ground (0V)
174	GND	Ground (0V)
175	DSI1_D0_N	Output Display1 D0 negative
176	HDMI0_TX1_P	Output HDMI0 TX1 positive
177	DSI1_D0_P	Output Display1 D0 positive
178	HDMI0_TX1_N	Output HDMI0 TX1 negative
179	GND	Ground (0V)
180	GND	Ground (0V)
181	DSI1_D1_N	Output Display1 D1 negative
182	HDMI0_TX0_P	Output HDMI0 TX0 positive
183	DSI1_D1_P	Output Display1 D1 positive
184	HDMI0_TX0_N	Output HDMI0 TX0 negative
185	GND	Ground (0V)
186	GND	Ground (0V)
187	DSI1_C_N	Output Display1 clock negative
188	HDMI0_CLK_P	Output HDMI0 clock positive
189	DSI1_C_P	Output Display1 clock positive
190	HDMI0_CLK_N	Output HDMI0 clock negative
191	GND	Ground (0V)
192	GND	Ground (0V)

193	DSI1_D2_N	Output Display1 D2 negative
194	DSI1_D3_N	Output Display1 D3 negative
195	DSI1_D2_P	Output Display1 D2 positive
196	DSI1_D3_P	Output Display1 D3 positive
197	GND	Ground (0V)
198	GND	Ground (0V)
199	HDMI0_SDA	Bidirectional HDMI0 SDA. Internally pulled up with a 2kΩ. 5V tolerant. (It can be connected directly to a HDMI connector; a small amount of ESD protection is provided on the Module by an on-board HDMI05-CL02F3)
200	HDMI0_SCL	Bidirectional HDMI0 SCL. Internally pulled up with a 2kΩ. 5V tolerant. (It can be connected directly to a HDMI connector; a small amount of ESD protection is provided on the Module by an on-board HDMI05-CL02F3)

Chapter 3. RDK X3 Module Boot Considerations

The RDK X3 Module can boot in two ways:

QSPI – normal operation

USB Recovery Mode – development and production programming

3.1 QSPI Boot

The RDK X3 Module normally boots from QSPI NAND. However, the QSPI's 64 MB of storage is not expected to contain all the files for a fully functioning system. Secondary storage needs to be provided through on-board eMMC or external Micro SD Card.

3.2 USB Recovery Mode

USB Recovery mode provides an alternate mode. In this mode, the system is connected to a host system and boots over QSPI Boot which can entry fastboot mode to burn in new fully functioning system. This is used when a new image needs to be flashed. To enter USB recovery mode, the nRPIBOOT * pin is held low when the system is powered on.

nRPIBOOT * is the SoC RCM0 strap

Only USB_DM/DP supports USB Recovery Mode

No other signals are required or supported for entering Force Recovery mode. If the force recovery strap is held low coming out of reset, RDK X3 Module will configure USB as a device and enter recovery mode.

See the USB section (Section 6.1) for an example figure that shows USB connected to a USB Micro B connector.

Chapter 4. Modular Connector

4.1 Module Connector Details

The RDK X3 Module connect to the carrier board using a 200-pin board-to-board connector. The mating connector used on the reference design carrier board will be listed in the RDK X3 Module AVL (Approved Validation List). The connector listed in the RDK X3 Module is the same, so that document can be referenced. This connector is a board-to-board Connector with 0.4mm Pitch, 1.45mm Height.

4.2 Module to Mounting Hardware

The RDK X3 Module is installed in the board-to-board connector to hold the board. In addition, it is recommended that the module is mounted to the main carrier board PCB using metal screws (or equivalent), both for mechanical integrity and to provide additional grounding points. And if install the heat sink or other thermal solution, the metal screws (or equivalent) are necessary. The recommended screws that match the metal hole on board are M2.0 × 4.0 mm typically, flat head. Other board-to-board connector heights are available. If a different height connector is used, the screw height will have to be adjusted accordingly to account for the difference in height from main carrier board PCB to module PCB.

4.3 Module Installation and Removal Operating Guidelines

To install the RDK X3 Module correctly, follow the sequence and mounting hardware instructions: Here are some suggested assembly guidelines.

1. Install the module

a). Start with baseboard that has suitable clearance room to match board-to-board connector height.

b). Insert module fully at an angle of 85-90 degree into the board-to-board connector.

c). Arc down the module board until the board-to-board d connector latch engages.

2. Assemble any required thermal solution on the module after the module has been installed correctly.

Figure 5-2. Module to Connector Assembly Diagram

（TBD）

To remove the module correctly, follow the installation sequence in reverse.

Chapter 5. Power

Power for the module is supplied on the +5V pins and is nominally 5.0V (see the RDK X3 Module Data Sheet for supply tolerance and maximum current).

! CAUTION: RDK X3 Module is not hot-pluggable. When installing the module, the main power supply should not be connected. Before removing the module, the main power supply (to VDD_IN pins) must be disconnected and allowed to discharge below 0.6V.

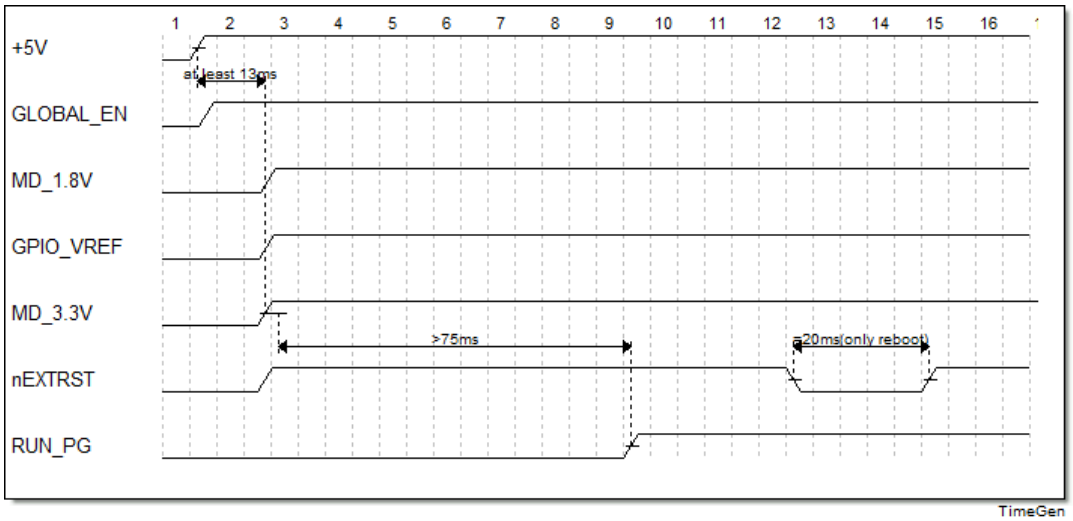
Table 5-1. Power and System Pin Descriptions

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK X3 Module Carrier Board	Direction	Pin Type
77,79,81,85,83,85,87	+5V	NA	Main power – Supplies PMIC and other regulators	Main DC input	Input	5.0V
104,106	+5V	NA	Main power – Supplies PMIC and other regulators, always NC；	Main DC input	Input	5.0V
93	nRPIBOOT	X3M_I2C4_SDA	A low on this pin forces booting from USB; if not used Leave floating. Internally pulled up via 4kΩ to +3.3V	System	Input	CMOS – 3.3V
92	RUN_PG	X3M_RESETN_IN	Module Reset. Reset to the module when driven low by the carrier board (only resets the SoC and eMMC device). Used as carrier board supply enable when pulled high by the module When module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. 4kΩ pull-up to 3.3V on the module.	System	Input	CMOS – 3.3V
99	GLOBAL_EN	NA	Input. Drive low to power off Module. Internally pulled up with a 47kΩ to +5V	System	Input	Open Drain, 5.0V

100	nEXTRST	X3M_RSTOUT_N	Output. An active-low reset output signal and generated by SOC watchdog timeout event. It is used to reset peripherals on the board, EMMC, Flash, Ethernet PHY, etc.	System	Output	CMOS – 3.3V

5.1. Power-up sequencing

The RDK X3 Module requires a single +5V power input and can supply up to 600mA at VDD_3V3 (Pin MD_3.3V) and VDD_1V8 (Pin MD_1.8V) to peripherals.
All pins should not have any power applied to them before the +5V rail is applied.
If the RDK X3 Module is to be booted using fastboot then RPI_nBOOT needs to be low within 2ms of +5V rising.
+5V should rise monotonically to 4.8V and stay above 4.8V for the entire operation of the RDK X3 Module.
The power-up sequence will start when both +5V rail is above 4.8V and GLOBAL_EN rises. GLOBAL_EN has internal RC delay so that it rises after +5V has risen. The order of events is as follows:
1. +5V rises, this is the main power input.
2. GLOBAL_EN rises, this is the enable of power supply of the module. After +5V rises, it must be kept high.
3. MD_3.3V rises, the VDD_3V3 output from the module. This voltage should rises at least 13ms after +5V risen.
4. RUN_PG rises at least 75ms after MD_3.3V, the reset signal of X3 SOC and PMIC chip. When the system finish bring up, it will be kept high.
Figure 5-1 Power-Up sequencing



Note: MD_3.3V and MD_1.8V are produced by the Power unit on the module. It is no need to input these power from external.

GPIO_VREF should be kept with MD_1.8V or MD_3.3V simultaneously.

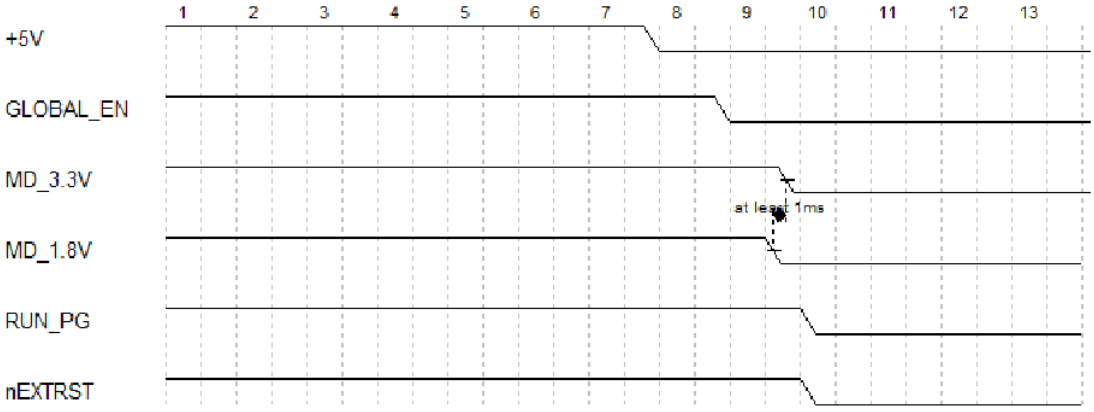
5.2. Power-down sequencing

The operating system should be shut down before the power is removed, to ensure that the file system remains consistent. If this can't be achieved, then a filesystem like btrfs, f2fs or overlayfs should be considered.

Once the operating system has shut down, the +5V rail can be removed or the GLOBAL_EN pin can be taken low to put the RDK X3 Module into the lowest power mode.

During the shutdown sequence the MD_1.8V will be discharged before the MD_3.3V rail.

Figure 5-2 Power-down sequencing



5.3. Power consumption

The exact power consumption of the RDK X3 Module will greatly depend on the tasks being run on the RDK X3 Module. The lowest shutdown power consumption mode is with the GLOBAL_EN driven low, typically is 50μA. With GLOBAL_EN high but software shut down, the typical consumption is 50mA. Idle power consumption is typically 200mA, but this varies considerably depending on the operating system. Operating power consumption is typically around 1.0A; again, this greatly depends on the operating system and the tasks being executed.

5.4. Regulator outputs

To make it easier to interface to the RDK X3 Module the on-board regulators (MD_3.3V and MD_1.8V) can each supply 600mA to devices connected to the RDK X3 Module. The loads on these outputs isn't taken into account in the power consumption figures.

Chapter 6. USB

RDK X3 Module allows multiple USB 2.0, USB 3.0, interfaces to be brought out of the module.

USB 3.0: 1x

See Table 6-1 for the supported USB 3.0 mapping options. These are the only options supported.

Pin #	Module Pin Name	X3 Signal	Usage and Description	Usage on RDK X3 Module Carrier Board	Direction	Pin Type
103	USB_N	USB_DM	USB 2.0 Data	USB conn/device/hub	Bidir	USB PHY
105	USB_P	USB_DP	USB 2.0 Data	USB conn/device/hub	Bidir	USB PHY
101	USB_OTG_ID	X3M_SD0_WPROT	For USB_ID function. 0 (low): SOC is USB host, perform USB host operation 1 (high): SOC is USB device.	USB ID	Input	CMOS – 3.3V
116	USB_RX_P	USB_RX_P	USB 3.0 Data	USB conn/device/hub	Bidir	USB PHY
118	USB_RX_N	USB_RX_M	USB 3.0 Data	USB conn/device/hub	Bidir	USB PHY
122	USB_TX_P	USB_TX_P	USB 3.0 Data	USB conn/device/hub	Bidir	USB PHY
124	USB_TX_N	USB_TX_M	USB 3.0 Data	USB conn/device/hub	Bidir	USB PHY
76	SD0_DET_N	X3M_SD0_DET_N	For USB Hot-Plug detect. when SOC is USB device.	USB conn/device/hub	Input	CMOS – 1.8V

Notes: In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.

6.1 USB

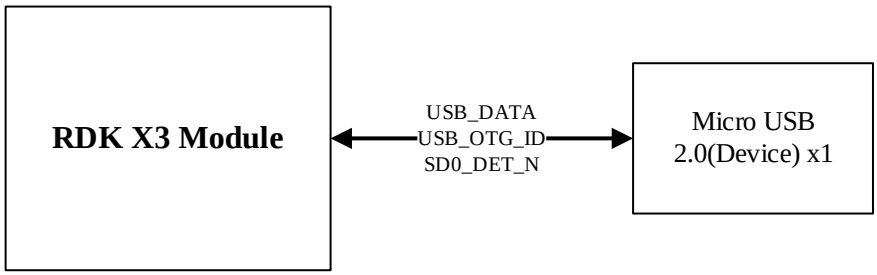
RDK X3 Module supports up to one USB 3.0 ports. And this port also can compatible USB2.0.

Note:

The example shown in Figure 6-1 is for connections to a USB device only connector to be used to support recovery mode (See Section 3.2 “USB Recovery Mode” for details on recovery mode) or a

USB device if booted normally. A USB Micro B connector is shown in the example.

Figure 6-1. USB Micro B USB Device and Recovery Connection Example



6.1.1 USB 2.0 Routing Guidelines

The following table details the requirements that apply to the USB 2.0 controller PHY interfaces: USB_DM/DP.

Table 6-2. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency (high speed): Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Min Pair to Pair spacing	Each pair should be separated by at least 3 times the signal trace width.		
Max loading: High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	Max loading should include any passive and active components on the trace such as CMC, Switch, ESD etc.
Reference plane	GND		
Trace impedance: Diff pair / SE)	90 / 45	Ω	±10%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Max trace length/delay With CMC or SW (Microstrip / Stripline) Without CMC or SW (Microstrip / Stripline	900/1050 (150) 1475/1720 (250)	mm(ps)	Prop delay assumption: 6.9/mm for stripline, 5.9ps/mm. for microstrip. See Note 3
Max intra-pair skew between USB_DM and USB_DP	3	ps	

Notes:

1. Up to four signal vias can share a single GND return via.

2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

3. CMC = Common-Mode-Choke. SW = Analog Switch.

6.1.2 USB 3.0 Routing Guidelines

USB_TX_P, USB_TX_M, USB_RX_P and USB_RX_M. Must be designed with a differential impedance of 90Ω±10%.

In order to minimize cross talk, it is recommended to keep high speed signals away from each other. Each pair should be separated by at least 5 times the signal trace width. Separating with ground as depicted will also help minimize cross talk.

Route all differential pairs on the same layer adjacent to a solid ground plane.

Do not route differential pairs over any plane split.

Adding test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test point are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.

Avoid 90°turns in trace. The use of bends in differential traces should be kept to minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135°. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.

Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for SuperSpeed differential pair signals and USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.

Match the etch lengths of the differential pair traces. There should be less than 5 mils difference between a SuperSpeed differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 25 mils relative trace length difference.

The etch lengths of the differential pair groups do not need to match, but all trace lengths should be minimized.

Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible the module connector

Chapter 7. Gigabit Ethernet

RDK X3 Module integrates a Realtek RTL8211F-CG Gigabit Ethernet controller. The magnetics and RJ45 connector would be implemented on the carrier board. Contact Realtek for carrier board placement and routing guidelines.

Table 7-1. Gigabit Ethernet Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK X3 Module Carrier Board	Direction	Pin Type

4	Ethernet_Pair1_P	GPHY_MDI1_P	GbE Transformer Data 1	Not assigned	Bidir	MDI
6	Ethernet_Pair1_N	GPHY_MDI1_N	GbE Transformer Data 1			
3	Ethernet_Pair3_P	GPHY_MDI3_P	GbE Transformer Data 3			
5	Ethernet_Pair3_N	GPHY_MDI3_N	GbE Transformer Data 3			
10	Ethernet_Pair0_N	GPHY_MDI0_N	GbE Transformer Data 0			
12	Ethernet_Pair0_P	GPHY_MDI0_P	GbE Transformer Data 0			
9	Ethernet_Pair2_N	GPHY_MDI2_N	GbE Transformer Data 2			
11	Ethernet_Pair2_P	GPHY_MDI2_P	GbE Transformer Data 3			
15	Ethernet_nLED3	PHY_nLED3	Ethernet 100Mbit Link LED		input	-
17	Ethernet_nLED2	PHY_nLED2	Ethernet 1Gbit Link LED		output	-

Notes: In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.

7.1Ethernet MDI Routing Guidelines

The following tables describes the Ethernet signal routing requirements and connections.

Table 7-2. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace impedance Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min trace spacing (pair-pair)	0.763	mm	
Max trace length/delay	109 (690)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Number of vias	minimum	Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.	

Notes: X3 SOC does not support delay or skewing of clock vs. data. This must be enabled in the PHY

Table 7-3. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
Ethernet_Pair [3:0]_N/P	DIFF I/O	Gigabit Ethernet MDI IF Pairs: Connect to Magnetics -/+ pins	
Ethernet_nLED3	O	510Ω (minimum) series resistor	Gigabit Ethernet Link LED: Connect to green LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS

Ethernet_nLED2	O	510Ω (minimum) series resistor	Megabit Ethernet Link LED: Connect to yellow LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS

Chapter 8. Display

RDK X3 Module Embedded designs can select from several display options including MIPI DSI and HDMI for external displays. The maximum number of simultaneous displays supported by RDK X3 Module is two.

8.1 MIPI DSI

RDK X3 Module supports three total MIPI DSI data lanes and a single clock lane. Each data lane has a peak bandwidth up to 1.5Gbps.

Table 8-1. DSI Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK X3 Module Carrier Board	Direction	Pin Type
187	DSI1_C_N	X3M_MIPI_DEV_CN	Display, DSI clock	Not assigned	Output	MIPI D-PHY
189	DSI1_C_P	X3M_MIPI_DEV_CP				
175	DSI1_D0_N	X3M_MIPI_DEV_D0N	Display, DSI data lane 0			
177	DSI1_D0_P	X3M_MIPI_DEV_D0P				
181	DSI1_D1_N	X3M_MIPI_DEV_D1N	Display, DSI data lane 1			
183	DSI1_D1_P	X3M_MIPI_DEV_D1P				
193	DSI1_D2_N	X3M_MIPI_DEV_D2N	Display, DSI data lane 2			
195	DSI1_D2_P	X3M_MIPI_DEV_D2P				
194	DSI1_D3_N	X3M_MIPI_DEV_D3N	Display, DSI data lane 3			
196	DSI1_D3_P	X3M_MIPI_DEV_D3P				

Notes: In the Type/Dir column, Output is from Module. Input is to Module. Bidir is for Bidirectional signals.

Notes: If EMI/ESD devices are necessary, they must be tuned to minimize impact to signal quality, which must meet the DSI spec. requirements for the frequencies supported by the design.

8.1.1 MIPI DSI and CSI Design Guidelines

Table 8-2 details the MIPI DSI and CSI interface signal routing requirements.

Parameter	Requirement	Units	Notes
Max frequency/data rate (per data lane)	405.5 / 811	MHz/Mbps	
Number of loads	1	load	
Reference plane	GND		
Trace impedance - Diff pair / SE	100 / 50	Ω	±10%
Via proximity (signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance. Loosely Coupled Diff. Pair recommended by Spec.
Inter-pair trace spacing - Microstrip / Stripline	4x / 3x	dielectric height	
Max PCB breakout length	5	mm	
Max trace delay 1 Gbps 1.5 Gbps	1100 800	ps	
Max intra-pair skew	1	ps	
Max trace delay skew between **DQ** and **CLK**	5	ps	DQ includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			

8.1.2 MIPI DSI and CSI Connection Guidelines

Table 8-3. MIPI DSI Signal Connections

Module Pin Name	Type	Termination	Description
DSI1_C_N/P	DIFF OUT	DSI Differential Clock: Connect to CLKn and CLKp pins of the primary DSI display	

DSI1_D[2:0]_N/P	DIFF OUT	DSI Differential Data Lanes 2:0: Connect to corresponding data lanes of DSI display.	

8.2 HDMI

A standard HDMI V1.4 interface is supported.

Table 8-4. HDMI Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on Horizon Robotics DevKit Carrier Board	Direction	Pin Type
184	HDMI0_TX0_N	HTX0N	HDMI data lane	Not assigned	Output	
182	HDMI0_TX0_P	HTX0P			Output	
178	HDMI0_TX1_N	HTX1N			Output	
176	HDMI0_TX1_P	HTX1P			Output	
172	HDMI0_TX2_N	HTX2N			Output	
170	HDMI0_TX2_P	HTX2P			Output	
190	HDMI0_CLK_N	HTXCN	HDMI clock lane		Output	
188	HDMI0_CLK_P	HTXCP			Output	
153	HDMI0_HPD	HHPD	HDMI Port Hot Plug Detect		input	
151	HDMI0_CEC	HCEC	HDMI CEC		Bidir	
200	HDMI0_SCL	HSCL	HDMI0 SDA. Internally pulled up with a 1.8kΩ. 5V tolerant		Bidir	
199	HDMI0_SDA	HSDA	HDMI0 SDA. Internally pulled up with a 1.8kΩ. 5V tolerant		Bidir	

Notes:

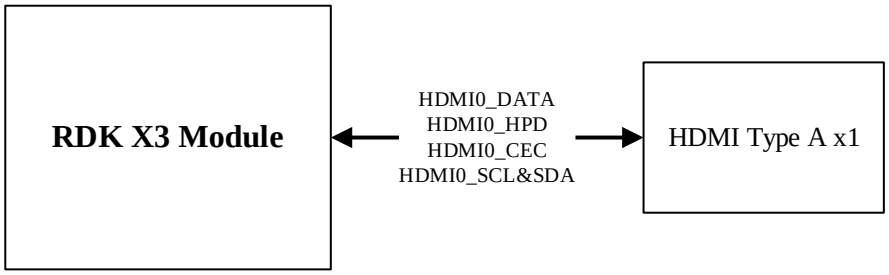
1. In the Type/Dir column, Output is from RDK X3 Module. Input is to RDK X3 Module. Bidir is for Bidirectional signals.

2. The directions for HHPD and HCEC are true when used for these functions. Otherwise as GPIOs, the direction is bidirectional

8.2.1 HDMI

This section shows the HDMI connection requirements, signal routing requirements, and topology.

Figure 8-1. HDMI Connection Example



Notes:

1. Level shifters required on DDC/HPD. X3 pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting. HPD level shifter on the RDK X3 Module is inverting.

Table 8-5. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Topology	Point to point		Unidirectional, differential
Termination At receiver On-board	100 500	Ω	Differential To 3.3V at receiver To GND near connector
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40	dB at DC dB at 3GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pair
Parameter	**Requirement**	**Units**	**Notes**
	<= -40	dB at 6GHz	
	IL/FEXT plot: See Figure 7-9		TDR plot: See Figure 7-10
Impedance			
Trace impedance - Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main

			route is an implementation option.
Reference plane	GND		
Trace spacing/Length/Skew			
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. See Note 1.
Trace spacing (pair-pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	3x 4x 5x to 7x	dielectric height	For Stripline, this is 3x of the thinner of above and below.
Trace spacing (Main link to DDC) Stripline Microstrip	3x 5x	dielectric height	For Stripline, this is 3x of the thinner of above and below.
Max total length/delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	63.5/2.5 (437) 50.8/2.0 (300) 63.5/2.5 (375)	mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max Total Length/Delay (Pre-1.4b - up to 165Mhz) Microstrip Stripline	254/10 (1500) 225/8.5 (1500)	mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See notes 1, 2, and 3
Max inter-pair (pair to pair) skew	150	ps	See notes 1, 2, and 3
Max GND transition via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	Y-pattern is recommended keep symmetry		Xtalk suppression is the best by Y pattern. Also, it can reduce the limit of pair-pair distance. Need review(NEXT/FEXT check) if via placement is not Y-pattern. See Figure 8-11

Minimum impedance dip	97 92	Ω@200ps Ω@35ps	
Recommended via dimension drill/pad Antipad via pitch	 200/400 840 880	 uM	
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of vias PTH via u-via	4 if all vias are PTH via Not limited if total channel loss meets IL sp		
Parameter	Requirement	Units	Notes
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check)
Topology			
The main route via dimensions should comply with the via structure rules (See via section)			See Figure 8-8
For the connector pin vias, follow the rules for the connector pin vias (See via section)			
The traces after main route via should be routed as 100Ω differential or as uncoupled 50ohm SE traces on PCB top or bottom.			
Max distance from RPD to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top: See Figure 7-12		Bottom: See Figure 8-13
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.

Placement PTH design Micro-via design	Place cap on bottom layer if main route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		See Figure 8-14
Pull-down Resistor (RPD), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		Placement: See Figure 8-15
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		
Choke between RPD and FET choke Max trace Rdc Max trace length	600 or 1 ≤20 4	Ω @ 100 MHz uH@DC-100 MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	GND/PWR void under/above cap is preferred		
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues) See Appendix A for details on CMC if implemented.			
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to GND)	0.35	pF	e.g. Texas Instruments TPD4E02B04DQAR
Footprint	Pad right on the net instead of trace stub		See Figure 8-16
Parameter	Requirement	Units	Notes
Location	After pull-down resistor/CMC and before RS		
Void	GND/PWR void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		See Figure 8-17
Series Resistor (RS) – Series resistor on N/P path for HDMI 2.0 (mandatory)			
Value	≤ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the RS value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	GND/PWR void under/above the RS device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		

Trace entering the SMT pad	One 45°	See Figure 8-18
Trace between components	Uncoupled structure	See Figure 8-19
HDMI connector		
Connector voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself	See Figure 8-20

Notes:

1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.

2. The average of the differential signals is used for length matching.

3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion

4. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

The following figures show the HDMI interface signal routing requirements.

Figure 8-9. IL and FEXT Plot

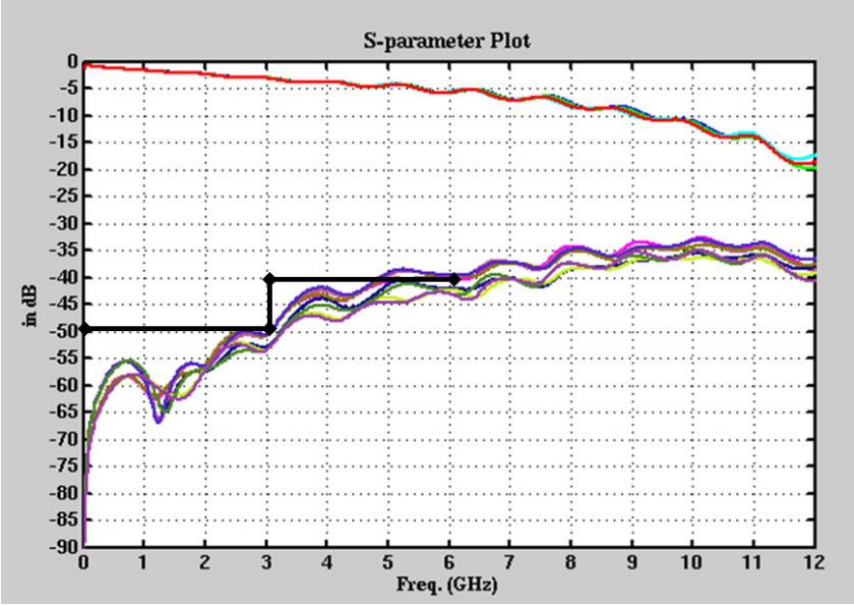


Figure 8-10. TDR Plot

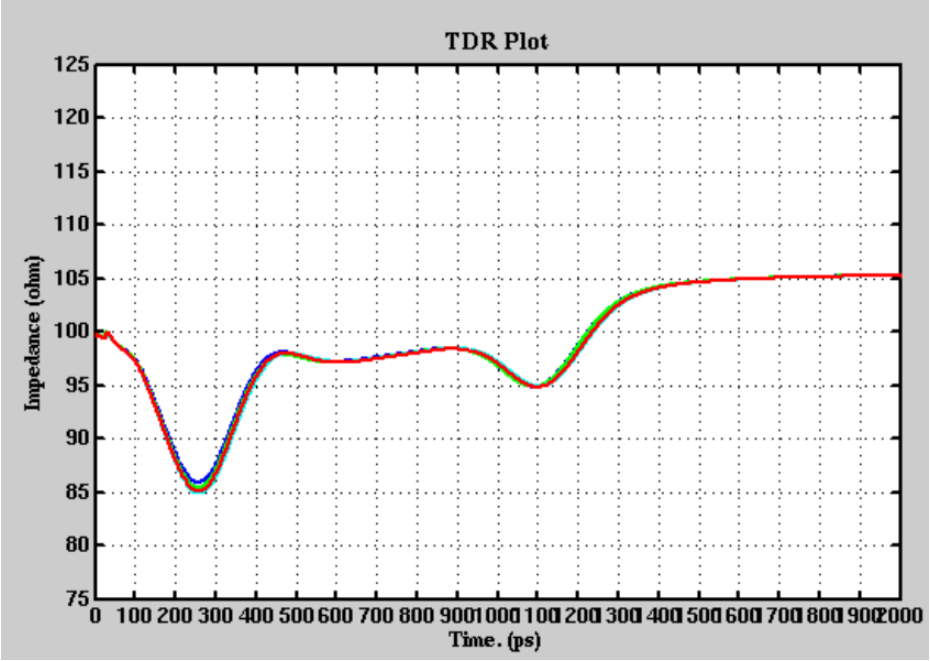


Figure 8-11. HDMI Via Topology

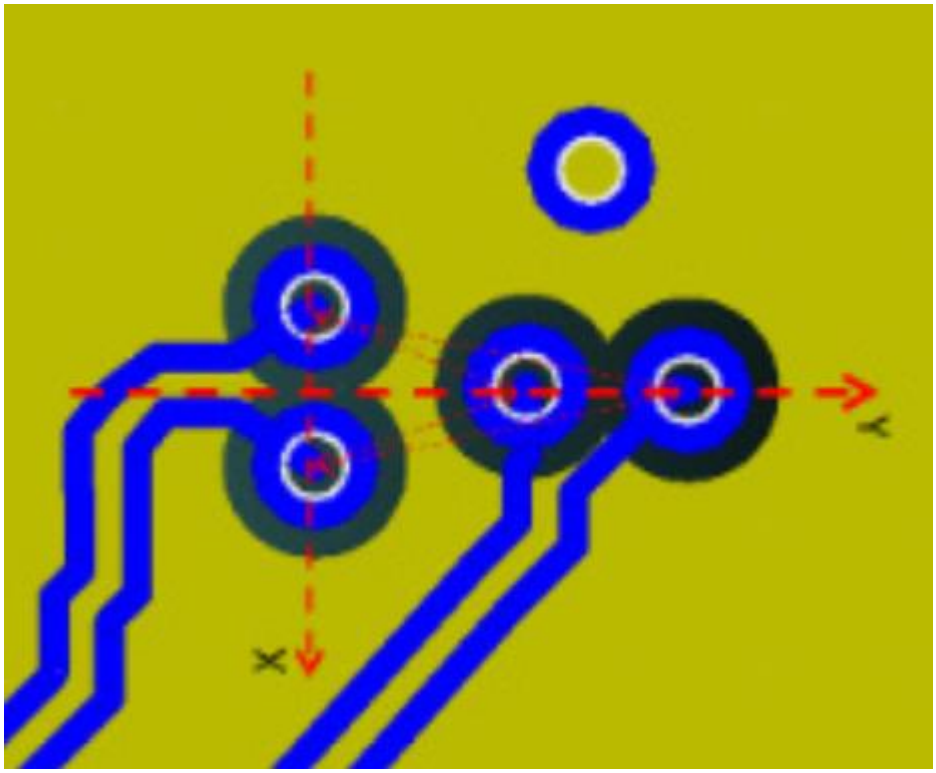


Figure 8-12. Add-on Components – Top

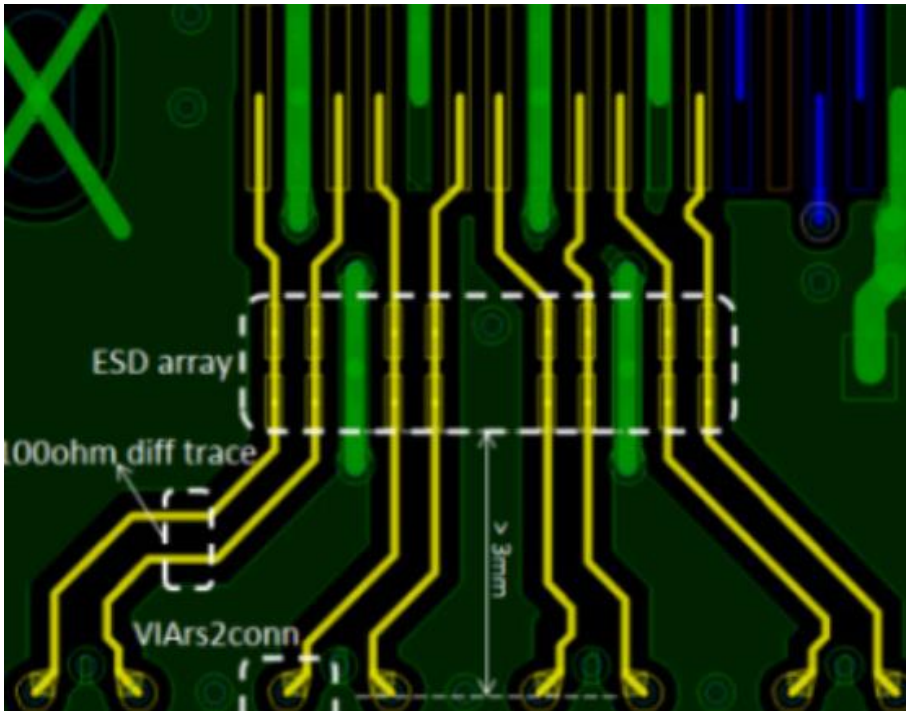


Figure 8-13. Add-on Components – Bottom

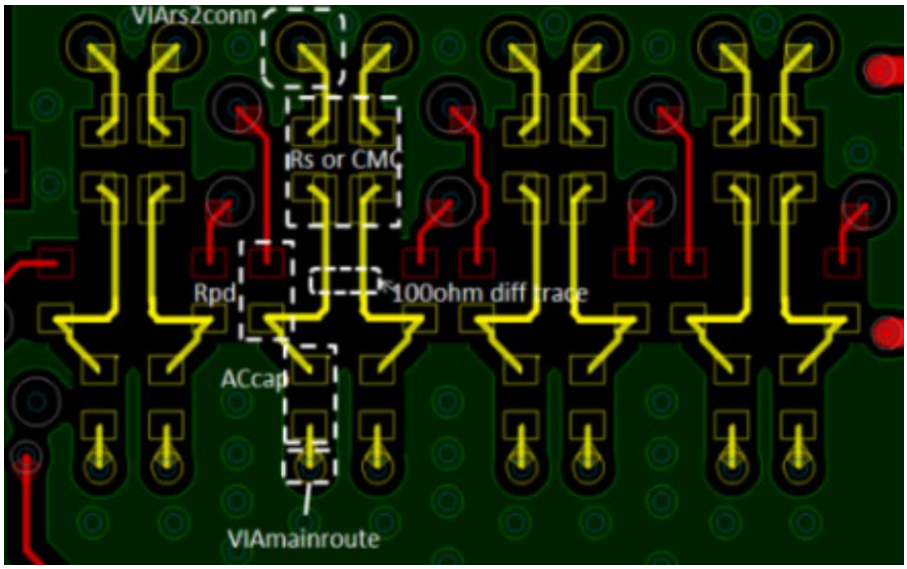


Figure 8-14. AC Cap Void


Figure 8-15. RPD, Choke, FET Placement

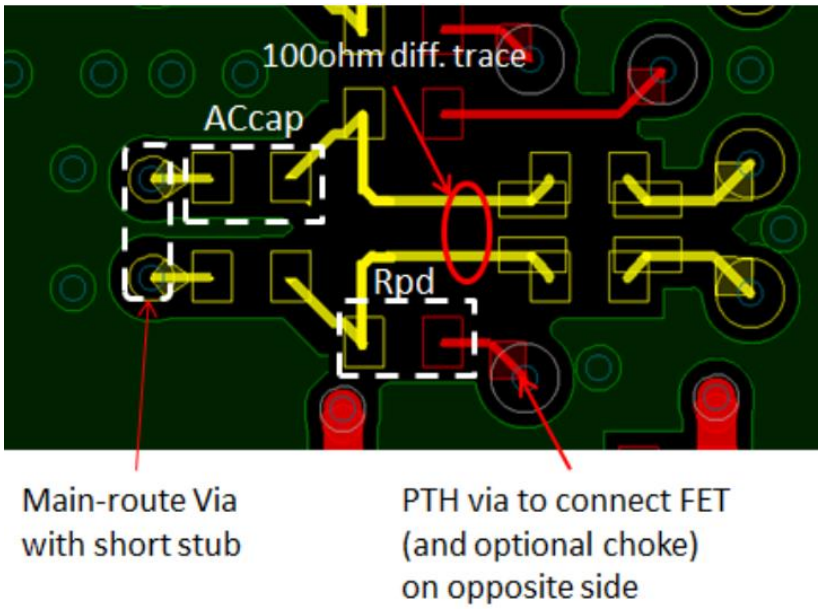


Figure 8-16. ESD Footprint

Figure 8-17. ESD Void

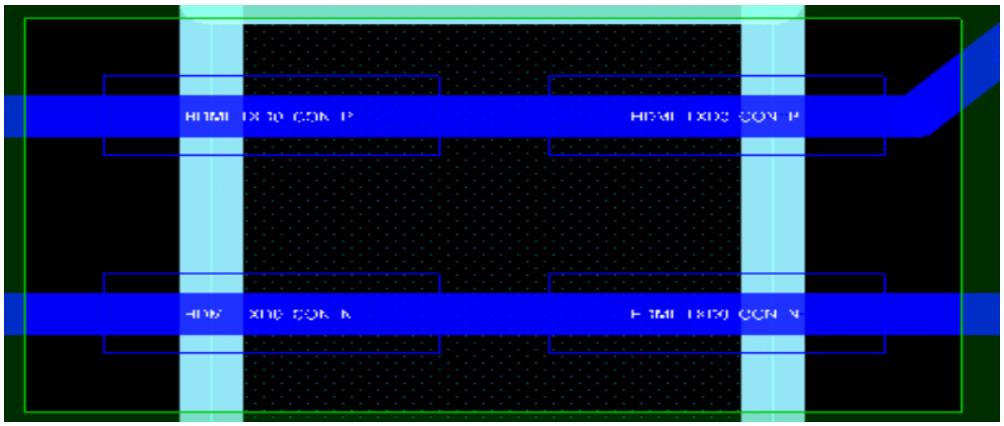


Figure 8-18. SMT Pad Trace Entering

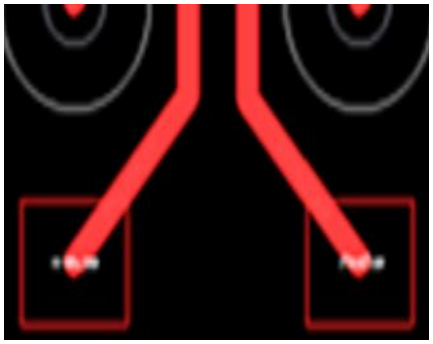


Figure 8-19. SMT Pad Trace Between

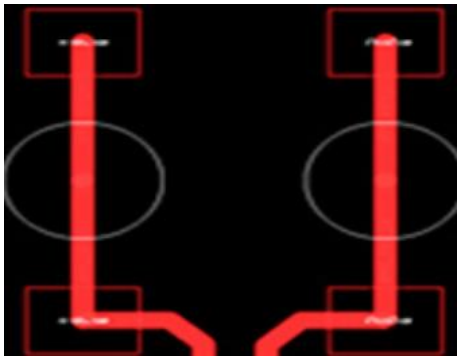
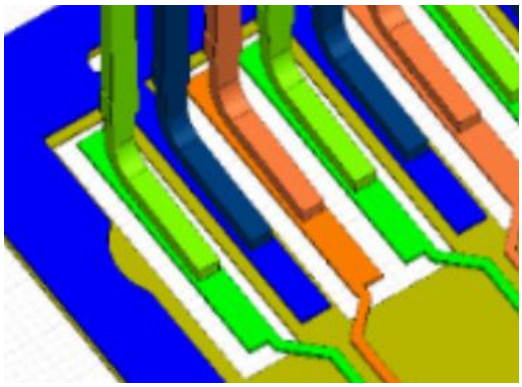


Figure 8-20. Connector Voiding



Chapter 9. MIPI CSI Video Input

RDK X3 Module brings eight MIPI CSI lanes to the connector. one quad-lane camera streams and two dual-lane camera streams c are supported. Each data lane has a peak bandwidth of up to 1.5 Gbps.

Note: In Table 9-1 and Table 9-2 the Direction column, the Output is from RDK X3 Module and the Input is to RDK X3 Module. Bidir is for bidirectional signals.

Table 9-1. CSI Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
140	CAM0_C_N	X3M_MIPI_HOST0_CN	Camera, CSI 0 Clock	Camera Connector #1	Input	MIPI D-PHY
142	CAM0_C_P	X3M_MIPI_HOST0_CP		Camera Connector #1		
128	CAM0_D0_N	X3M_MIPI_HOST0_D0N	Camera, CSI 0 Data 0	Camera Connector #1		
130	CAM0_D0_P	X3M_MIPI_HOST0_D0P		Camera Connector #1		

134	CAM0_D1_N	X3M_MIPI_HOST0_D1N	Camera, CSI 0 Data 1	Camera Connector #1		
136	CAM0_D1_P	X3M_MIPI_HOST0_D1P		Camera Connector #1		
115	CAM1_D0_N	X3M_MIPI_HOST1_D0N	Camera, CSI 1 Data 0	Not Assigned		
117	CAM1_D0_P	X3M_MIPI_HOST1_D0P				
121	CAM1_D1_N	X3M_MIPI_HOST1_D1N	Camera, CSI 1 Data 1			
123	CAM1_D1_P	X3M_MIPI_HOST1_D1P				
127	CAM1_C_N	X3M_MIPI_HOST1_CN	Camera, CSI 1 Clock	Camera Connector #2		
129	CAM1_C_P	X3M_MIPI_HOST1_CP				
133	CAM1_D2_N	X3M_MIPI_HOST3_D0N	Camera, CSI 1 Data 2			
135	CAM1_D2_P	X3M_MIPI_HOST3_D0P				
139	CAM1_D3_N	X3M_MIPI_HOST3_D1N	Camera, CSI 1 Data 3			
141	CAM1_D3_P	X3M_MIPI_HOST3_D1P				
169	CAM2_C_N	X3M_MIPI_HOST2_CN	Camera, CSI 2 Clock	Not Assigned		
171	CAM2_C_P	X3M_MIPI_HOST2_CP				
157	CAM2_D0_N	X3M_MIPI_HOST2_D0N	Camera, CSI 2 Data 0			
159	CAM2_D0_P	X3M_MIPI_HOST2_D0P				

Notes: In the Type/Dir column, Output is from RDK X3 Module. Input is to RDK X3 Module. Bidir is for Bidirectional signals.

Table 9-2. Miscellaneous Camera Pin Descriptions

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
35	ID_SC	X3M_SPI2_SCLK	I2C3 SCLK	Camera I2C Clock. 1kΩ pull-up to 3.3V on the Carrier Board	Bidir	Open Drain – 3.3V
36	ID_SC	X3M_SPI2_CSN	I2C3 SDA	Camera I2C Data. 1kΩ pull-up to 3.3V on the Carrier Board	Bidir	Open Drain – 3.3V
80	SCL1	X3M_I2C1_SCL	I2C1 SCLK	Camera I2C Clock. 4kΩ pull-up to 3.3V on the Module	Bidir	CMOS – 3.3V
82	SDA1	X3M_I2C1_SDA	I2C2 SDA	Camera I2C Data. 4kΩ pull-up to 3.3V on the Module	Bidir	CMOS – 3.3V
56	GPIO3	X3M_I2C0_SCL	I2C2 SDA	Camera I2C Data. 2kΩ pull-up to Vref on the Module	Bidir	Open Drain – 3.3/1.8V

58	GPIO2	X3M_I2C0_SDA	I2C1 SCLK	Camera I2C Clock. 2kΩ pull-up to Vref on the Module	Bidir	Open Drain – 3.3/1.8V
97	Camera_GPIO	X3M_WKUPIN_N	Camera Reset or GPIO	Camera Connector #0,1,2	Output	CMOS – 3.3V

Notes:

1. In the Type/Dir column, Output is from RDK X3 Module. Input is to RDK X3 Module. Bidir is for Bidirectional signals.

9.1 CSI Design Guidelines

CSI routing and connection requirements are shown as table 9-3.

Table 9-3. MIPI CSI D-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of loads	1	load	
Reference plane	GND		
Trace impedance: Diff pair / SE	90-100 / 45-50	Ω	±10%
Via proximity (signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance.
Trace spacing: Microstrip / Stripline	2x / 2x	dielectric	
Max PCB breakout delay	48	p	
Max Insertion loss 1 Gbps 1.5 Gbps 2.5 Gbps	3.00 2.90 1.92	dB	
Max trace delay / length 1 Gbps (Stripline/Microstrip) 1.5 Gbps 2.5 Gbps	2526 (421) / 2487 (421) 1913 (319) / 1885 (319) 900 (150) / 886 (150)	ps (mm)	
Max intra-pair skew	1	ps	
Max trace delay skew between DQ and CLK 1 / 1.5 / 2.5 Gbps	40 / 26.7 / 16	ps	DQ includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface,

			or 4 differential data lanes for a x4 interface
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in Figure 8-1. Any EMI/ESD solution must be compatible with the frequency required by the design.

Table 9-4. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[2:0]_CLK_N/P	I	See Note	CSI Differential Clocks. Connect to clock pins of camera. See Table 8-3 for details
CSI[2:0]_D[1:0]_N/P	I/O	See Note	CSI Differential Data Lanes: Connect to data pins of camera. See Table 8-3 for details

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in Figure 8-1. Any EMI/ESD solution must be compatible with the frequency required by the design.

Chapter 10. Audio

RDK X3 Module supports I2S audio interfaces.

Table 10-1. Audio Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
25	PCM_DOUT	X3M_I2S0_SDO	I2S Audio Port Data Out	Expansion Header	Output	CMOS – 3.3V
26	PCM_FS	X3M_I2S0_LRCK	I2S Audio Port Left/Right Clock		Bidir	CMOS – 3.3V
27	PCM_DIN	X3M_I2S1_SDI	I2S Audio Port Data In		Input	CMOS – 3.3V
49	PCM_CLK	X3M_I2S0_BCLK	I2S Audio Port Clock		Bidir	CMOS – 3.3V
54	GPIO4	X3M_I2S0_MCLK	I2S Audio Port 0 Master Clock		Bidir	CMOS – 3.3V

Notes:

1. In the Type/Dir column, Output is from RDK X3 Module Input is to RDK X3 Module. Bidir is for Bidirectional signals.
2. If the pin PCM_CLK and PCM_FS used as GPIO function both, one of them at least should be configured input direction via software.

Table 10-2. Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / device organization	1	load	
Max loading	8	pF	
Reference plane	GND		
Breakout region impedance	Min width/spacing		
Trace impedance	50	Ω	±20%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note
Trace spacing - Microstrip or Stripline	2x	dielectric height	
Max trace length/delay	~22 (3600)	In (ps)	
Max trace length/delay skew between SCLK and SDATA_OUT/IN	~1.6 (250)	In (ps)	

Note: Up to four signal vias can share a single GND return via.

Chapter 11. Miscellaneous Interfaces

11.1 I2C

RDK X3 Module brings four I2C interfaces to the connector pins. CAM_I2C is included in Table 11-1. The assignments in the I2C interface mapping table should be used where applicable for the I2C interfaces.

Table 11-1. I2C Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
35	ID_SC	X3M_SPI2_SCLK	General I2C 3 Clock. None pull-up resistor on module.	Expansion Header	Bidir	CMOS – 3.3V/1.8V
36	ID_SD	X3M_SPI2_CSN	General I2C 3 Data. None pull-up resistor on module.	Expansion Header	Bidir	CMOS – 3.3V/1.8V
56	GPIO3	X3M_I2C0_SCL	General I2C 0 Clock. 1kΩ pull-up to Vref on the module.	Expansion Header	Bidir	CMOS – 3.3V/1.8V
58	GPIO2	X3M_I2C0_SDA	General I2C 0 Data. 1kΩ pull-up to Vref on the module.	Expansion Header	Bidir	CMOS – 3.3V/1.8V
80	SCL1	X3M_I2C1_SCL	General I2C 1 Clock. 4kΩ pull-up to 3.3V on the module.		Bidir	CMOS – 3.3V
82	SDA1	X3M_I2C1_SDA	General I2C 1 Clock. 4kΩ pull-up to 3.3V on the module.		Bidir	CMOS – 3.3V

Notes:

1. In the Type/Dir column, Output is from RDK X3 Module Input is to RDK X3 Module. Bidir is for Bidirectional signals.

2. The directions for I2C0 and I2C3 are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

11.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to RDK X3 Module do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the read/write bit removed or 8-bit including the read/write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format).

Notes:

• The RDK X3 Module I2C0 interfaces have 1kΩ pull-ups on the module. Pads for additional pullups are recommended in case a stronger pull-up is required due to additional loading on the interfaces. If the communicate show the error，the frequency should be modified to 100kbps.

• The RDK X3 Module I2C1 interfaces have 4kΩ pull-ups on the module. If the communicate show the error， the frequency should be modified to 100kbps.Show as the table below, when the external resistor is not suitable, the Vol will not be low enough to meet the requirement.

Table 1. TXS0108E Pullup Results Summary

RESISTOR VALUE (kΩ)	V_{OL} (V)	V_{OH} (V)
No external resistor	0.029	3.18
4.7	*0.264*	3.19
9.8	*0.169*	3.19
47	0.059	3.19
100	0.038	3.19

• The RDK X3 Module I2C3 interfaces have none pull-ups on the module. Pads for additional pullups are necessary in case a stronger pull-up is required due to additional loading on the interfaces. If the communicate show the error，the frequency should be modified to 100kbps.

Table 11-2. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency - Standard-mode / Fm / Fm+	100 / 400	kHz	See Note 1
Topology	Single ended, bi-directional, multiple initiators and targets		
Max loading - Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	GND or PWR		
Trace impedance	50 – 60	Ω	±15%
Trace spacing	1x	dielectric height	
Max trace length/delay Standard Mode Fm, Fm+ Modes	3400 (~20) 1700 (~10)	ps (in)	

Notes:

1. Fm = Fast-mode, Fm+ = Fast-mode Plus.

2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.

3. No requirement for decoupling caps for PWR reference.

11.2 SPI

The RDK X3 Module brings out two of the X3 SOC SPI interfaces.

Table 11-4. SPI Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
35	ID_SC	X3M_SPI2_SCLK	SPI 2 Clock	Expansion Header	Bidir	
36	ID_SD	X3M_SPI2_CSN	SPI 2 Chip Select		Output	CMOS – 3.3V
48	GPIO27	X3M_SPI2_MISO	SPI 2 Initiator In and Master Out		Input	CMOS – 3.3V
27	GPIO20	X3M_SPI2_MOSI	SPI 2 Initiator Out and Target In		Output	CMOS – 3.3V
38	GPIO11	X3M_JTG_TCK	SPI 1 Clock		Bidir	CMOS – 3.3V
39	GPIO8	X3M_JTG_TMS	SPI 1 Chip Select		Output	CMOS – 3.3V
40	GPIO9	X3M_JTG_TDO	SPI 1 Initiator In and Master Out		Output	CMOS – 3.3
44	GPIO10	X3M_JTG_TDI	SPI 1 Initiator Out and Target In		Input	CMOS – 3.3V

Note:1． In the Type/Dir column, Output is from RDK X3 Module Input is to RDK X3 Module. Bidir is for Bidirectional signals.

2. The directions for SPI[2:1]x are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

11.2.1 SPI Design Guidelines

Table 11-5. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency	48	MHz	
Configuration / device organization	4	load	
Max loading (total of all loads)	15	pF	

Reference plane	GND		
Breakout region impedance	Minimum width and spacing		
Max PCB breakout delay	75	ps	
Trace impedance	50	Ω	±10%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note
Trace spacing - Microstrip / Stripline	4x / 3x	dielectric height	
Max trace length/delay (PCB main trunk – For MOSI, MISO, SCK & CS) Point-point 2x-load star/daisy	195 (1228) 120 (756)	mm (ps)	
Max trace length/delay (Branch-A) for MOSI, MISO, SCK and CS 2x-load star/daisy	75 (472)	mm (ps)	
Max trace length/delay skew from MOSI, MISO and CS to SCK	16 (100)	mm (ps)	At any point

Note: Up to four signal vias can share a single GND return via.

11.3 UART

The RDK X3 Module brings three UARTs out to the main connector. See Table 11-6 for typical assignments of the three available UARTs.

Table 11-6. UART Pin Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
16	Debug_Uart0_RX	X3M_UART0_RXD	UART #0 Receive	Debug_UART	Input	CMOS – 1.8V
18	Debug_Uart0_TX	X3M_UART0_TXD	UART #0 Transmit. Buffered on module to keep connected devices from affecting state of the pin during power-on as it is one of the SoC strap pins	Debug_UART	Output	CMOS – 1.8V
64	UART2_TXD	UART2_TXD	UART #2 Transmit.	Expansion Header	Output	CMOS – 3.3V/1.8V

68	UART2_RXD	UART2_RXD	UART #2 Receive	Expansion Header	Input	CMOS – 3.3V/1.8 V
51	GPIO15	X3M_UART3_RXD	UART #3 Receive	Expansion Header	Input	CMOS – 3.3V/1.8 V
55	GPIO14	X3M_UART3_TXD	UART #3 Transmit.	Expansion Header	Output	CMOS – 3.3V/1.8 V

Note:1． In the Type/Dir column, Output is from RDK X3 Module Input is to RDK X3 Module. Bidir is for Bidirectional signals.

2. The directions for UART[3:2]x are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

11.4 Debug

RDK X3 Module supports a UART and JTAG for debugging purposes. The UART intended for debug is UART0 with is routed to a level shifter then to a 3-pin header on the developer kit carrier board. JTAG is routed to a 40-pin header on the developer kit carrier board.

Table 11-9. JTAG and Debug UART Description

Pin #	Module Pin Name	X3 Signal	Usage/Description	Usage on RDK Carrier Board	Direction	Pin Type
28	GPIO13	X3M_JTG_TRSTN	JTAG reset input, low active,default	Expansion Header	Input	CMOS – 3.3V/1.8 V
38	GPIO11	X3M_JTG_TCK	JTAG test clock		Bidir	CMOS – 3.3V/1.8 V
39	GPIO8	X3M_JTG_TMS	JTAG test mode select		Bidir	CMOS – 3.3V/1.8 V
40	GPIO9	X3M_JTG_TDO	JTAG test data Out		Output	CMOS – 3.3V/1.8 V
44	GPIO10	X3M_JTG_TDI	JTAG test data In		Input	CMOS – 3.3V/1.8 V
16	Debug_Uart0_RX	X3M_UART0_RXD	UART #0 Receive		Input	CMOS – 1.8V
18	Debug_Uart0_TX	X3M_UART0_TXD	UART #0 Transmit. Buffered on module to keep connected devices from affecting state of the	Debug_UART	Output	CMOS – 1.8V

			pin during power-on as it is one of the SoC strap pins			

Notes:

1．In the Type/Dir column, Output is from RDK X3 Module Input is to RDK X3 Module. Bidir is for Bidirectional signals.

2. The directions for JTAG are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

11.4.1 Debug UART

The UART0 interface is intended to be used for debug purposes.
Table 11-10. Debug UART Connections

Module Pin Name	Type	Termination	Description
Debug_Uart0_TX	O	UART #0 Transmit: Connect to RX pin of serial device	
Debug_Uart0_RX	I	If level shifter implemented, 100kΩ to supply on the non-RDK X3 Module side of the device.	UART #0 Receive: Connect to TX pin of serial device

Chapter 12. Revision History

Version	Date	Description
v1.0	2023.05.23	first version